Claims

[c1] 1. A memory device, comprising

a substrate;

a gate oxide layer, disposed on a surface of the substrate;

a gate, disposed on a portion of the gate oxide layer;

a buried drain line, located in the substrate beside both sides of the gate;

a spacer, disposed on sidewalls of the gate;

a deep doped region, located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device;

an insulation layer, disposed above the bit line; and

a word line, disposed above the gate and the insulation layer, perpendicular to a direction of the bit line.

[c2] 2. The memory device of claim 1, wherein the insulation layer is formed with silicon oxide.

[c3] 3. The memory device of claim 1, wherein the spacer is formed with silicon oxide.

[c4] 4. The memory device of claim 1, wherein the word line is formed with a material comprising polysilicon.

[c5] 5. The memory device of claim 1, wherein the deep doped region is located in the substrate beside both sides of the spacer.

[c6] 6. A fabrication method for a memory device, comprising:

forming a gate oxide layer on a substrate;

forming a bar-shaped conductive structure on the gate oxide layer, wherein a cap layer is formed on a top of the bar-shaped conductive structure;

forming a buried drain line in the substrate beside both sides of the bar-shaped conductive structure;

forming a spacer on sidewalls of the bar-shaped conductive structure and the cap layer;

forming a deep doped region in the substrate beside both sides of the spacer,

wherein the buried drain line and the deep doped region together form a bit line of the memory device;

forming an insulation layer above the bit line;

removing the cap layer;

forming a conductive layer on the substrate; and

patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line and a plurality of gates.

[c7] 7. The method of claim 6, wherein there is an etching selectivity between the cap layer and the spacer.

[c8] 8. The method of claim 6, wherein there is an etching selectivity between the cap layer and the insulation layer.

[c9] 9. The method of claim 6, wherein the cap layer is formed with a material comprising silicon nitride.

[c10] 10. The method of claim 6, wherein the spacer is formed with a material comprising silicon oxide.

[c11] 11. The method of claim 6, wherein an insulation layer is formed with a material comprising silicon oxide.

[c12] 12. The method of claim 6, wherein forming the buried drain line includes performing an ion implantation process using the cap layer and the bar-shaped conductive structure as an implantation mask.

[c13] 13. The method of claim 6, wherein the deep doped region is formed by performing an ion implantation process using the cap layer and the spacer as an implantation mask.

[c14] 14. The method of claim 6, wherein forming the insulation layer above the bit line comprises:

forming globally an insulation material on the substrate, the insulation layer covers the cap layer; and

removing a portion of the insulation material until the cap layer is exposed.

[c15] 15. The method of claim 14, wherein removing the portion of the insulation material includes performing back etching or chemical mechanical polishing.

[c16] 16. The method of claim 6, wherein forming the bar-shaped conductive structure and the cap layer comprises:
forming sequentially a conductive layer and a material layer on the gate oxide layer; and
patterning the material layer and the conductive layer to form the bar-shaped conductive structure and the cap layer.

[c17] 17. The method of claim 6, wherein forming the spacer comprises:
forming a conformal silicon layer on the substrate; and
back-etching the conformal silicon oxide layer to form the spacer.